

1 Overview

DP32020A is a serial decoder row driver chip designed for LED scanning screens. It integrates a serial decoder circuit that prevents multiple channels from being turned on at the same time, which can prevent 3 or more channels from being turned on at the same time, causing excessive channel current and burning the chip. DP32020A can completely replace the original 3-8 decoder (74HC138) circuit of the LED module, more effectively simplifying the complexity of the LED module PCB wiring, thereby improving the overall image effect of the display.

2 Features

ÿ Operating voltage 3.5V~5.5V ÿ Integrated

serial decoding circuit to prevent multiple channels from being turned on at

the same time ÿ Support 3-scan~64-scan scanning screen (does not support static screen and 2-

scan screen) ÿ Integrated 8-channel power PMOS tube

- OUT_MAX = 3.5A @ VDD = 5.0V -

RON=110mÿ@VDD=5.0V&IOUT=1.0A

ÿ Maximum power consumption < 600 mW @ VDD = 5.0V ÿ Integrated

adaptive shadow cancellation function to effectively eliminate line smearing $\ddot{\textbf{y}}$

Shadow cancellation potential can be configured by register to adapt to more complex environments

ÿ Improve the cross-line phenomenon of the display screen caused by LED open circuit ÿ Simplify the complexity of LED module PCB wiring ÿ Packaging form: SOP16, QFN4*4-16L ÿ ESD ÿ 8KV

3 Application areas

ÿ High refresh rate LED video display ÿ

Single color, dual color, full color LED display

ÿ High density, small pitch LED light board display

4 Circuit Schematic Diagram

4.1 Input and output equivalent circuit

DIN, DCK, RCK input terminals

OUT0~7 Output terminal



DOUT Output

FSM Discharging Current FSM Discharging Current Machine Translated by Google



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4.2 Internal circuit diagram





DP320202P3265S

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Revision History

Version	Revision Date Rev	vision by	Revisions			
V1.0	2022.09		Initial release			
V1.1	2022.09	СҮС	1. Modify the AC electrical characteristics content			
			2. Added AC electrical characteristics timing diagram			
V1.2	2022.10	СҮС	1. Added QFN4*4-16L package			
V1.3	2022.11	СҮС	1. Modify the packaging information			
V2.0	2023.06	WM	1. Update document structure 2. Modify the internal functional block diagram 3. Optimization suggestion application circuit content 4. Optimize the timing diagram in the data sheet			
V2.1	2024.01	WM 1. Modify	he input and output equivalent circuit			
V2.2	2024.01	WM	Modify line break control and fading time A Modify register configuration			
V2.3	2024.05	WM 1. Modify	egister configuration			
Developer Microelectron.						

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5 Product Description

ÿ Pin definition



ÿ Pin Description

SOP16 Pin No. QFN4*4-16L	Pin No. Pin Name		Pin Description
1ÿ11	1	VDD	Power Input
2	2	FROM	Data Entry
3	3	DCK	Serial signal clock input
4	4	RCK	Blanking register configuration clock input
5~8ÿ13~16	5~8ÿ13~16	OUT0~OUT7 OUT Output	
9	e	GND	land
10	10	DOUT serial data ou	put
12	11ÿ12	NC	Empty feet

ÿ Product ordering information

Product Name	Package	Package Packing Quantity/Plate		Moisture sensitivity level	
DP32020A	SOP16	method	4000		
	QFN4*4-16L	Taping	5000	MSL=3	

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ÿ Product marking



DP32020A is the product name

BXXXXXX represents the product batch number



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6 Recommended application circuit

LED scanning screens are widely used in indoor display screens to reduce costs. However, the parasitic capacitance of the LED anode will instantly generate a discharge path when scanning and switching, causing the display screen to have a smearing phenomenon. Users can use the DP32020A with a discharge circuit function and refer to the scanning screen recommended application circuit as shown below, and match it with the constant current driver chip DP5125 with a built-in pre-charging function, so that the upper and lower smearing phenomenon can be completely eliminated.

Because DP32020A is an 8-channel output integrated power chip, in order to avoid excessive heat accumulation, it is recommended to use it in displays with more than 16 scans, and pay attention to the temperature conditions

during use



LED display 16 scan application diagram

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7 Parameters

7.1 Maximum Limit Parameters

project	symbol	Rating	unit
Supply voltage	VCC	0~6.0	In
Input voltage (all pins)	COME	-0.4~VDD+0.4	In
OUT terminal continuous working current	ID	-2.5	A
OUT terminal instantaneous maximum current	IOUT_MAX	-3.5	A
Power loss	PD	<600	mW
Package thermal resistance	Rth(j-a)	80	ÿ/W
Operating temperature	Topr	-40~85	ÿ
Storage temperature	Test	-40~150	ÿ
HBM Human Body Model	VESD	ÿ8	KV

ÿ All voltage values are based on the chip ground (GND) as the reference point, and the test temperature of the maximum limit parameters is 25ÿ.

ÿ If the actual working conditions exceed the specified values, it may cause permanent damage to the components; if the actual working conditions are slightly lower than the maximum values and work for a long time, it may reduce the performance of the components.

The above are only some of the specified values, and this product does not support functional operation under other conditions outside the specifications.

ÿThe maximum peak temperature of surface mount products cannot exceed 260ÿ. The temperature curve is based on the J-STD-020 standard, the actual factory conditions and the solder paste manufacturer's recommendations.



7.2 Recommended working range

project	symbol	Test conditions	Min Typ M	ax Unit		
Supply voltage	VCC	-	3.5	5.0	5.5	In
Output voltage (DOUT)	VDOUT	-	0.7 — V	DD		In
Output current (DOUT)	ЮН	VOH =VDD -0.5V	— -16 -	_	?). ??	m.a.
	IOL	VOL =0.5V	— 20 —			
Input voltage	HIV		0.7 VDD —	- VDD		ln.
(DIN,DCK,RCK)	WILL	VDD-0.0V-0.0V	0	— 0.3VI	סכ	

ils

7.3 DC Electrical Characteristics (VDD=5.0V)

project	symbol	Test conditions	Min Typ M	ax Unit		
Logic supply voltage	VDD	ele	3.0	5.0	5.5	In
Power supply current	IDD_OFF	All OUT outputs set low — 400 -	— uA			
Gate turn-on voltage	VGS(th)	VDS=VGS,ID=250uA — -0.7			-0.9	In
Source-drain on-resistanc	e RDS(on)[1:7]	VGS=-5.0V, IOUT=-2.0A — 110			130 mÿ	
High level	Р ніv		0.7 VDD —	- VDD		
Input voltage	WILL	Logic potential	0	— 0.3 V	(DD	In
20						



7.4 Dynamic Characteristics (Unless otherwise specified, VDD=3.5Vÿ5V, Ta=25ÿ)

project	symbol	Test conditions	Min Typ Max	Unit	
Output rise delay	tPLH			50	ns
Output falling delay	tpHL	VDD=5.0V CL=12pF		100	 ns
Output rising edge	tr			60	ns
Output falling edge	tf			400	ns
Build Time	tst		30		ns
Keep Time	thd	ic	30		ns

8 Timing Waveform



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9 Line feed control and fading time

DP32020A is a common anode display serial decoding line tube driver. Each line change is fixed to send 1 DCK, and the channel output is high valid; the input data DIN to the output data

The rising edge interval of DOUT is fixed at 8 DCK.

symbol		describe	Minimum	Maximum
Tshadow The blanking time is equal		The blanking time is equal to the DCK high level width	n 500ns	. 2
	Setup	Setup time	60ns	, XIO
	Thold	Hold time	60ns	101
	换行 → ← Thold	换行 换行 →	—_Tline——→	换行
	DIN ⊢ Tsetup		.65	
C	оск0	1	2 n	0
	LINE_0			
	LINE 1			
j	.INE			
	lelor	2°.		
	Oer			



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10 Register Configuration

DP32020A has built-in 4-bit registers:

BIT Na	ame Default Value	describe						
3	VR_UP[2] 1'b1	The highest bit in the pull-up cancellation circuit reference potential configuration register VR_UP[2:0]						
2	reserved 1'b0							
		The reference potential of the pull-up cancellation circuit ca	n be configured as (Vdd=5V) according to the register VR_UF	[2:0] - the				
		0000ÿVdd*7/20 =1.75V	1000 ÿVdd*11/20 =2.75V	default value is 3.25V. The data pin corresponds to				
1:0 VF	R_UP[1:0] 2'b10	0001ÿVdd*8/20 =2.0V	1001 ÿVdd*12/20 =3.0V	DIN, which corresponds to the C signal of 3-8				
		0010ÿVdd*9/20 =2.25V	1010ÿVdd*13/20 =3.25V 1011 ÿ	decoding. DCK corresponds to the A signal of 3-8				
		0011ÿVdd*10/20 =2.5V	Vdd*15/20 =3.5V	decoding. RCK corresponds to the B signal of 3-8 decode				

The way to configure the register is: When DCK is low, 8 clocks (4 dummy clocks + 4 register configuration clocks) are sent to RCK.

During the 4 clocks of register configuration, register data is sent via DCK.





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11Package size



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QFN4*4-16L



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12Important Statement

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