DP3264S 16 channels 64 sweep low transition PWM constant current source driver

1 Overview

DP3264S is a common anode 16-channel low-turnover PWM constant current driver chip designed specifically for LED displays. It integrates high-precision current generation circuit technology on-chip, so that the current error between chips can be controlled within 2.0%. It also integrates a variety of exclusive technologies to enhance the display effect of LED displays, which can bring more improvements to the display.

2 Features

ÿ Power supply voltage range: 3.5ÿ5.5V ÿ

Operating temperature range: -40ÿÿ85ÿ ÿ Scan

range: 1ÿ64 scans, adjustable ÿ 16 constant current

output channels ÿ Constant current output

range

- 0.5mAÿ20mA

ÿ Channel-to-channel current

error - Typical value: ±1.2% Maximum value: ±2.0% ÿ

Chip-to-chip current error -

Typical value: ±0.2% Maximum value: ±2.0% ÿ High gray

independent display, high display refresh rate ÿ

Optimize display state -

Improve low gray uniformity

- Improve the first row dark phenomenon

- Improve the upper and lower

ghosting phenomenon - Improve

high and low gray coupling

- Improve cross-board coupling ÿ Integrated PLL generates

internal GCLK, lower EMI ÿ Package: QSOP24/

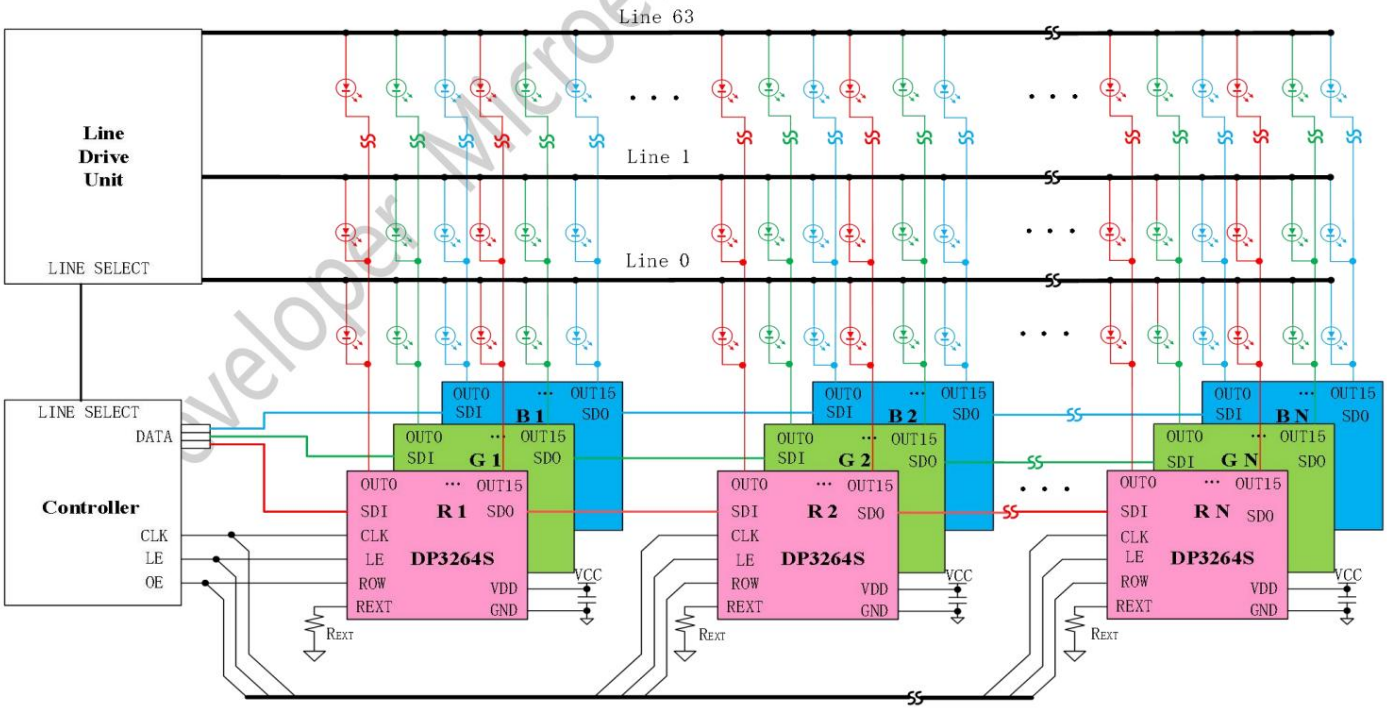
QFN24 ÿ Excellent ESD characteristics

3 Application areas

ÿ High refresh rate LED video display ÿ

Single color, dual color, full color LED display

ÿ High density, small pitch LED light board display



DP3264S Typical Application Schematic

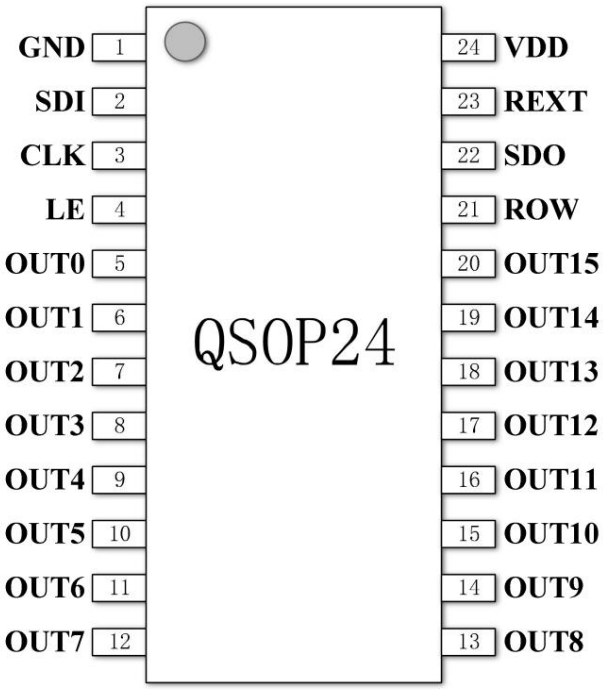
Table of contents

Revision History

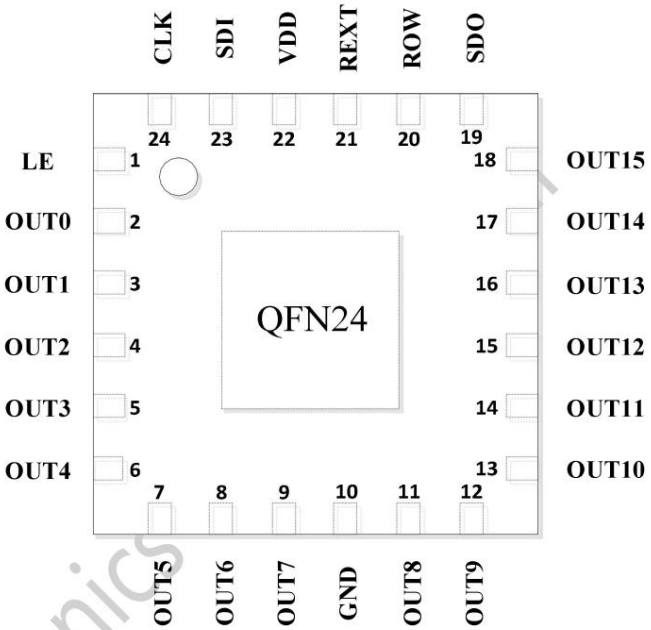
Version Revision	Date Revision by		Revisions
V1.0	2022.07	GYC Initial version	
V2.0	2023.05	WM	Update document structure Add the following content: 1. Chip version description 2. Test circuit diagram 3. Timing waveform 4. Typical characteristic diagram 5. Some sample images of display effects 6. Instructions and Registers 7. Package heat dissipation power 8. Load terminal voltage

4 Product Description

ÿ Pin definition



QSOP24 pin definition diagram



QFN24 pin definition diagram

ÿ Pin Description

QSOP24 Pin Number QFN24 Pin Number	Pin Name	Pin Description
1 10	GND	Chip ground terminal
2 23	SDI	Serial data input
3 24	CLK	Serial clock input
4 1	THE	The latch end of data and instructions. Different LE lengths represent different instructions.
5ÿ20	2ÿ9 11ÿ18 OUT0ÿOUT15 Constant current output terminal	
21 20	ROW	Line feed signal
22 19	SDO	Serial data output
23 21	RULE	Connect to external resistor
24 22	VDD	Chip power supply

QSOP24 Pin Description

ÿ Product ordering information

Product Name	Package	Packing	Quantity/Plate	Moisture sensitivity level
DP3264S	QSOP24	method	4000	MSL=3
	QFN24	Taping	5000	

ÿ Product marking

QSOP24

QFN24

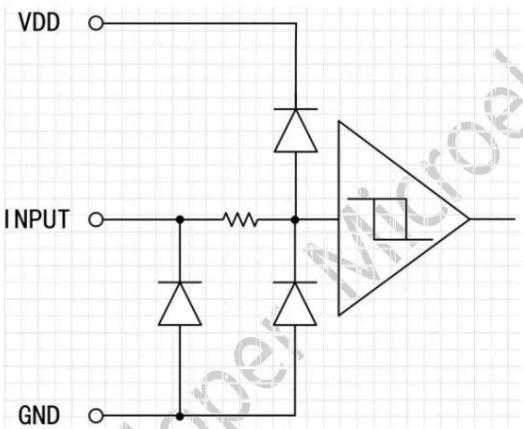
DP3264S is the product name

XXXXXX represents the product batch number

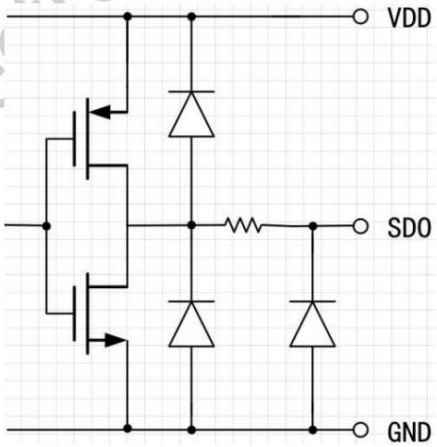
5 Circuit Schematic Diagram

5.1 Input and output equivalent circuit

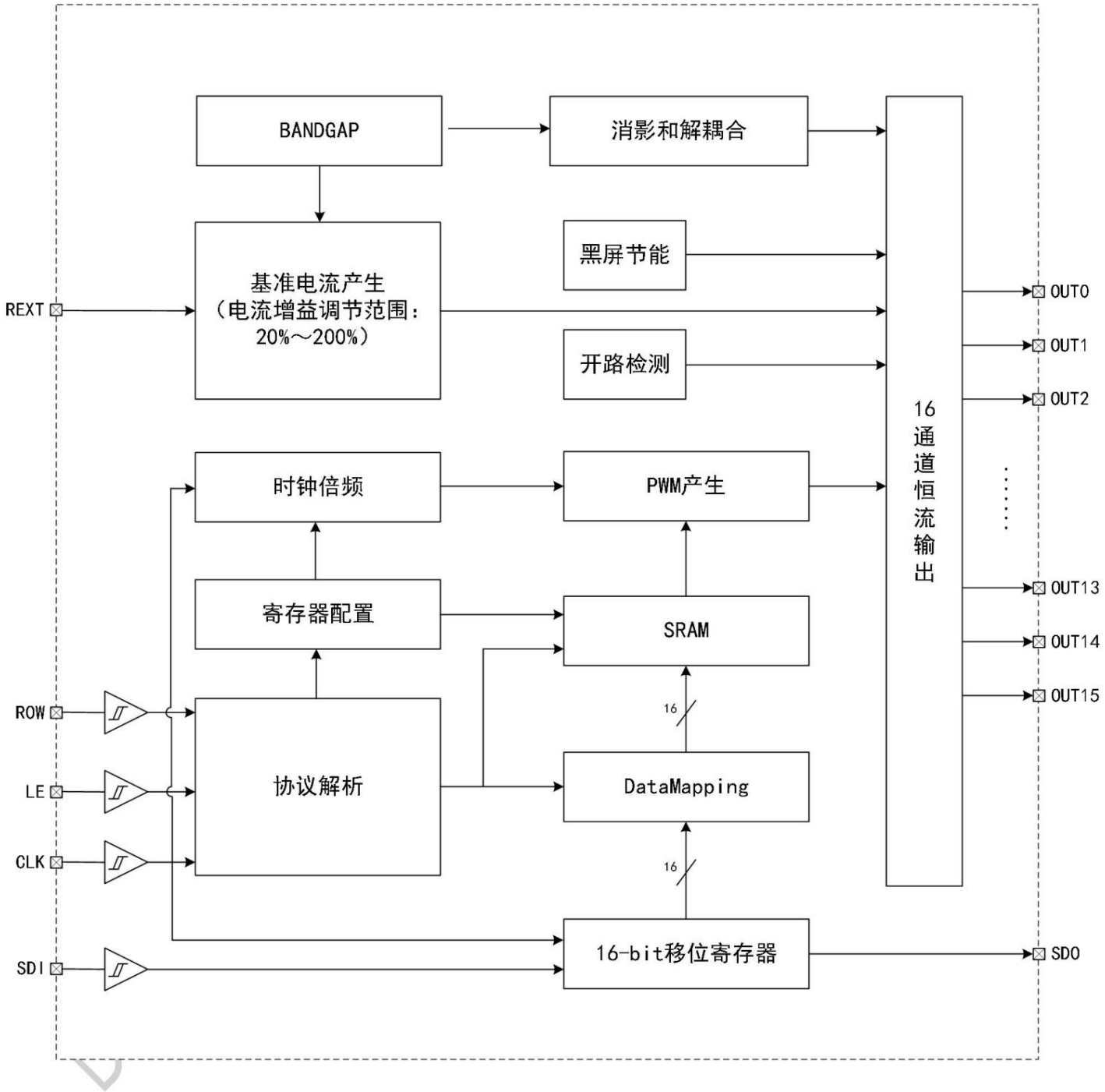
SDI, CLK, LE, OE input terminal



SDO output



5.2 Internal Circuit Diagram



Internal circuit diagram

6 Parameter table

6.1 Maximum Limit Parameters

project	symbol	Rating	unit
Power supply	VDD	0 ÿ 6	In
voltage Output	IT	20	m.a.
current Input	COME	-0.4 ÿ VDD+0.4	In
voltage Output withstand voltage	VOUT	11	In
Clock frequency	FCLK	25	MHz
Operating temperature	Topr	-40 ÿ 85	ÿ
Storage temperature	Test	-55 ÿ 150	ÿ

ÿ All voltage values are based on the chip ground (GND) as the reference point, and the test temperature of the maximum limit parameters is 25ÿ.

ÿ If the actual working conditions exceed the specified values, it may cause permanent damage to the components; if the actual working conditions are slightly lower than the maximum values and work for a long time, it may reduce the performance of the components.

The above are only some of the specified values, and this product does not support functional operation under other conditions outside the specifications.

ÿ The maximum peak temperature of surface mount products cannot exceed 260ÿ. The temperature curve is based on the J-STD-020 standard, the actual factory conditions and the solder paste manufacturer's recommendations.

Factory set.

6.2 ESD Level

6.2.1 Exposure to ESD

symbol	condition		Min Typ Max	Unit		
V(ESD)	Human body discharge model ÿHBMÿ1	OUTn Pin-GND	·	±8	·	kV
		OTHER Pin-GND	·	±8	·	kV
	Machine Model (MM) 2	OUTn Pin-GND	·	±0.4	·	kV
		OTHER Pin-GND	·	±0.4	·	kV

ÿ [1] The minimum HBM model ESD voltage of all pins complies with the Class-3B standard of JEDEC JS-001-2017 document.

ÿ [2] The minimum MM model ESD voltage of all pins complies with the Class-C standard of JEDEC EIA/JESD22-A115C document.

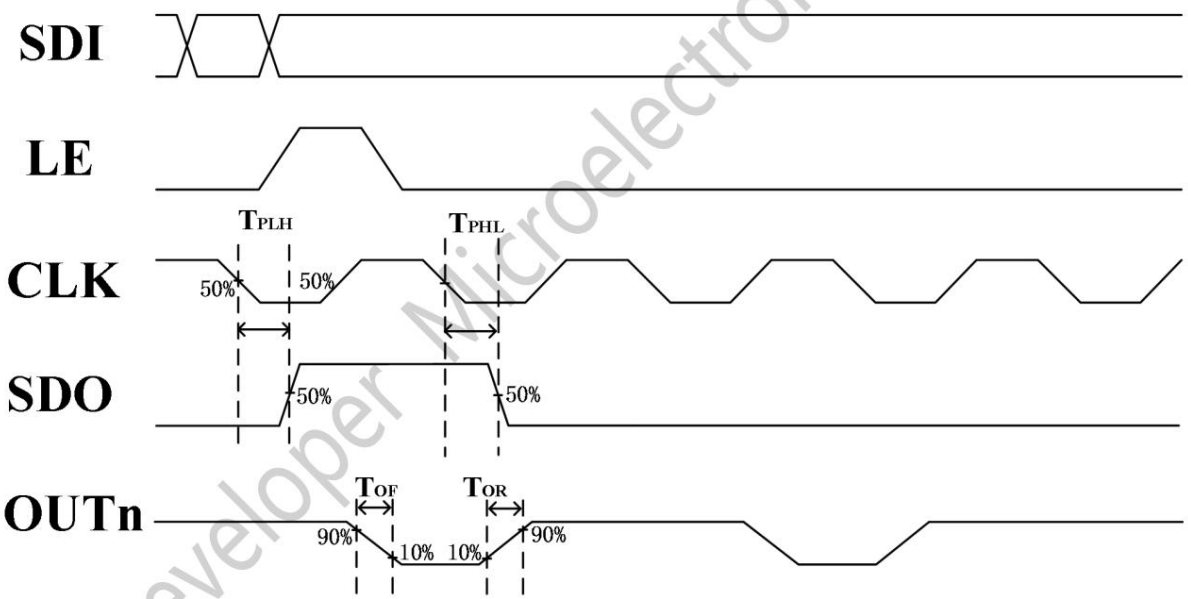
6.3 Electrical Characteristics (Unless otherwise specified, VDD=3.5Vÿ5V, Ta=25ÿ)

project	Symbol	Test Circuit	Test conditions		Min	Typ	Max	Unit
REXT Voltage Characteristics	VR_TT	1	VDD=5V,REXT=1K IGAIN=100%,Ta=25ÿ		1.499	1.513	1.526	In
	VR_LT		VDD=5V REXT=1K IGAIN=100%	Ta=-40ÿ	·	1.501	·	In
	VR_HT			Ta=85ÿ	·	1.521	·	In
	VR_LV		Ta=25ÿ REXT=1K IGAIN=100%	VDD=5.5V	·	1.516	·	In
	VR_HV			VDD=3.5V	·	1.510	·	In
Constant current output inflection point	VOUT1	2	IOUT=18mA		·	420	·	mV
	VOUT2		IOUT=9mA		·	382	·	mV
	VOUT3		IOUT=4.5mA		·	360	·	mV
Output current error between chips DCHIP		2	VDS=0.6V		—	±0.2		± 2.0 %
Output current error between channels DCHL		2	VDS=0.6V		—	± 0.7		±2.0 %
Constant current error/ VDS variation	%/D VDS	2	VDS=0.3~3.0V		—	— ± 1.0		%/V
Constant current error/VDD change	%/D VDD	2	VDD=3.5V~5.0V		—	— ± 1.0		%/V
Output voltage when ON VO(ON)		2	OUT0~OUT15		0.3	·	VDD	In
SDO Driver Current	High level IOH	3	VDD=5V		—	-22	—	mA
	Low Level IOL				—	23	—	mA
Output level high level VOH		4	IOH=-1mA		4.6	—	—	In
	Low level VOL		IOL=1mA		—	—	0.4	In
High level logic input voltage VIH		5	·		0.7*VDD	·	VDD	In
Low level logic input voltage VIL			·		GND	·	0.3*VDD	V
Supply Current (White screen power consumption)	IDD1	6	REXT=3K, white screen IOUT=6mA, refresh rate 3840		·	5.2	·	m.a.
Supply Current (Black screen for energy saving)	IDD3	6	REXT=3K, black screen IOUT=6mA, performance first		·	3.82	·	m.a.
	IDD4		REXT=3K, black screen IOUT=6mA, low power consumption first		·	1.61	·	m.a.
	IDD5		REXT=3K, black screen IOUT=6mA, extremely low power consumption		·	0.7	·	m.a.

6.4 Dynamic Characteristics (Unless otherwise specified, VDD=3.5Vÿ5V, Ta=25ÿ)

project	Symbol	Test Circuit	Test conditions	Min	Typ	Max	Unit
CLK-SDO Delay	TPHL	7	VDD=5Vÿ FDCLK=12.5MHz	-	-	50	ns
CLK-SDO Delay	TPLH		VDD=5Vÿ FDCLK=12.5MHz	-	-	50	ns
Constant current output rise time tOR			IOUT=10mAÿ ÿVOUT=3V	-	-	45	ns
Constant current output fall time tOF			IOUT=10mAÿ ÿVOUT=3V	-	-	35	ns

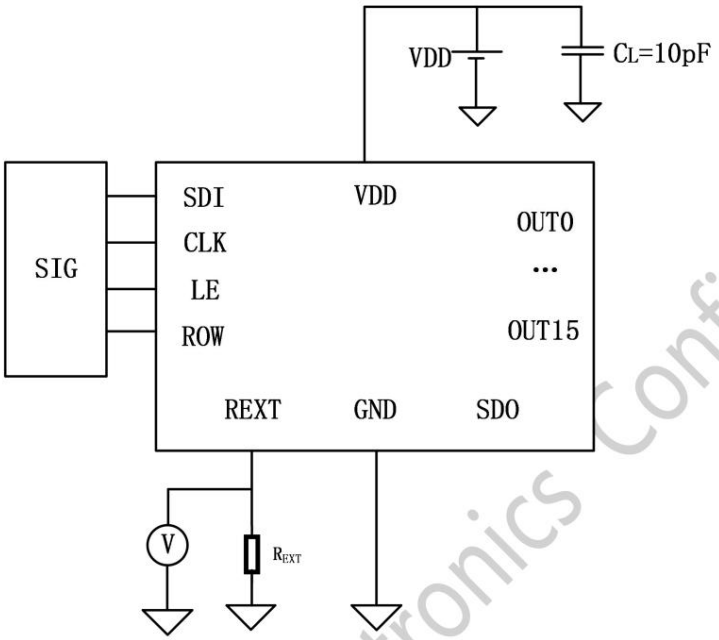
7 Timing Waveform



8 Test circuit diagram

8.1 Test Circuit 1

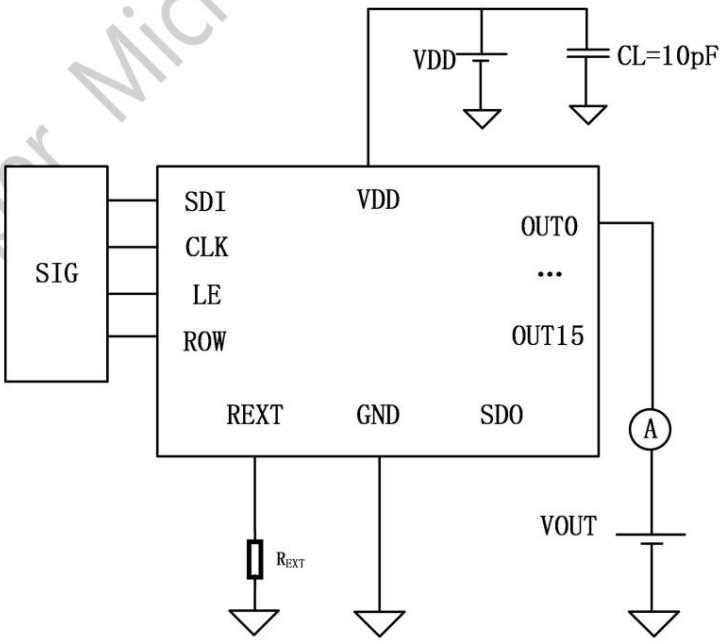
ÿ External resistor voltage



Test circuit 1 schematic diagram

8.2 Test Circuit 2

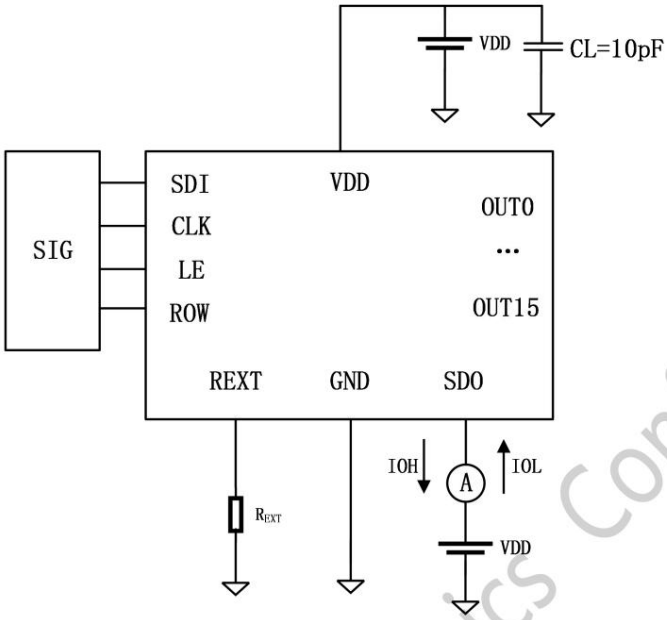
ÿ Constant current output inflection point voltage & corresponding inflection point current (under open circuit detection state)



Test circuit 2 schematic diagram

8.3 Test Circuit 3

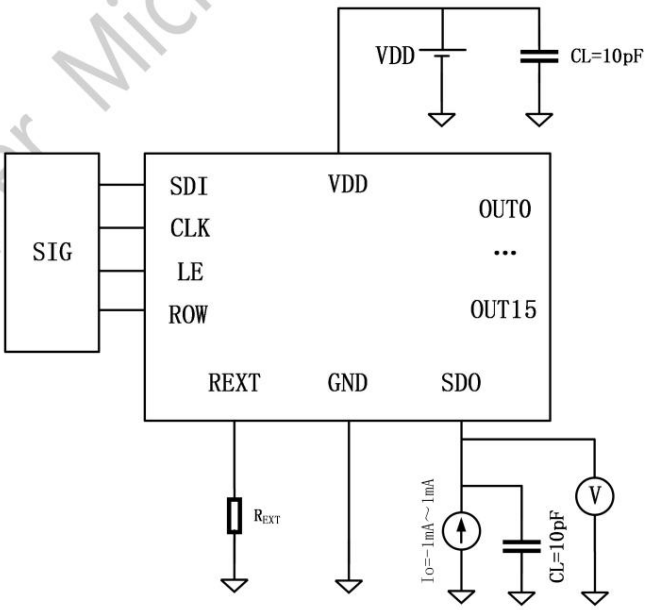
ÿ IOHÿIOL



Test circuit 3 schematic diagram

8.4 Test Circuit 4

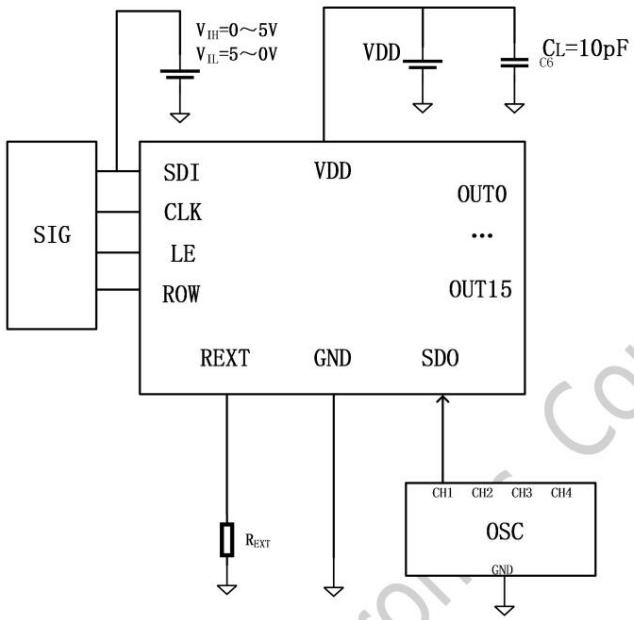
ÿ VOHÿVOL



Test circuit 4 schematic diagram

8.5 Test Circuit 5

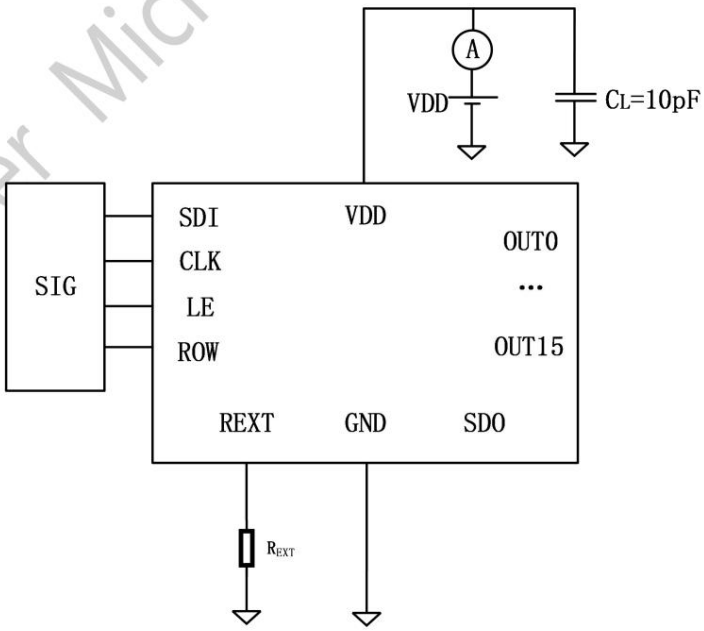
ÿ VIHÿVIL



Test circuit 5 schematic diagram

8.6 Test Circuit 6

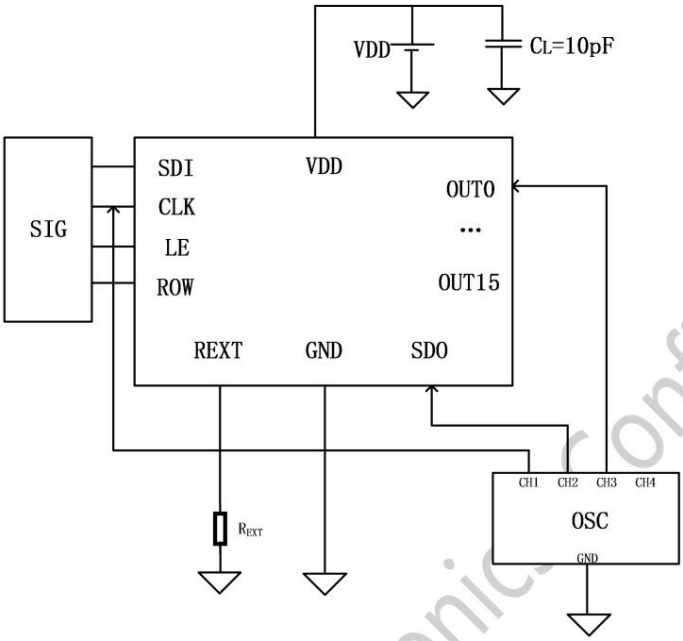
ÿ Power supply current



Test circuit 6 schematic diagram

8.7 Test Circuit 7

ÿ Dynamic characteristics

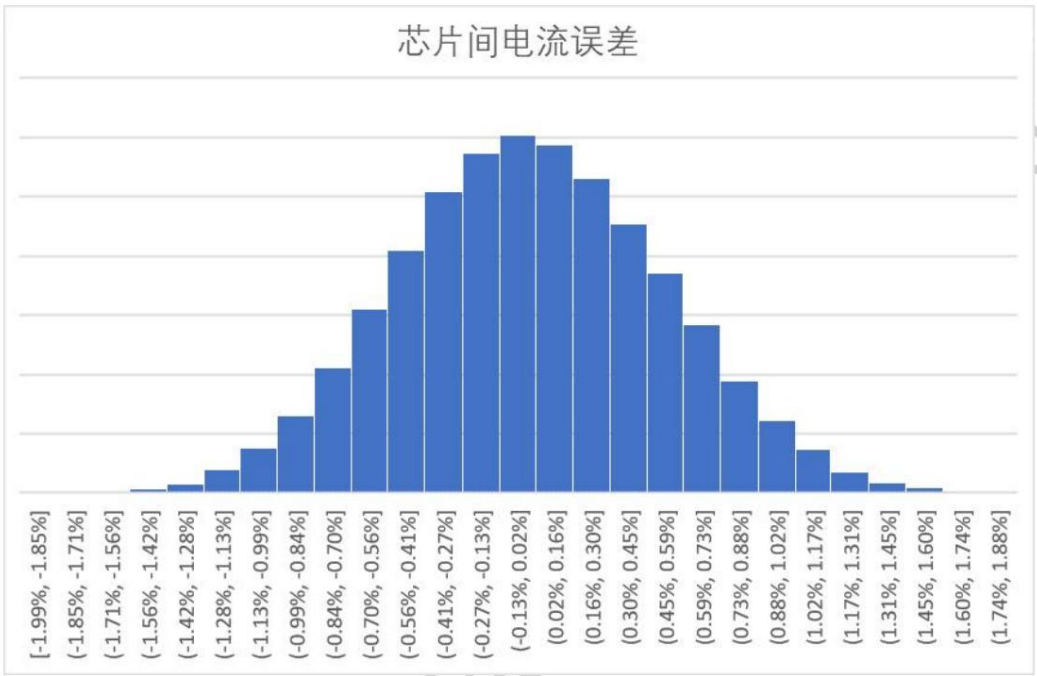


Test circuit 7 schematic diagram

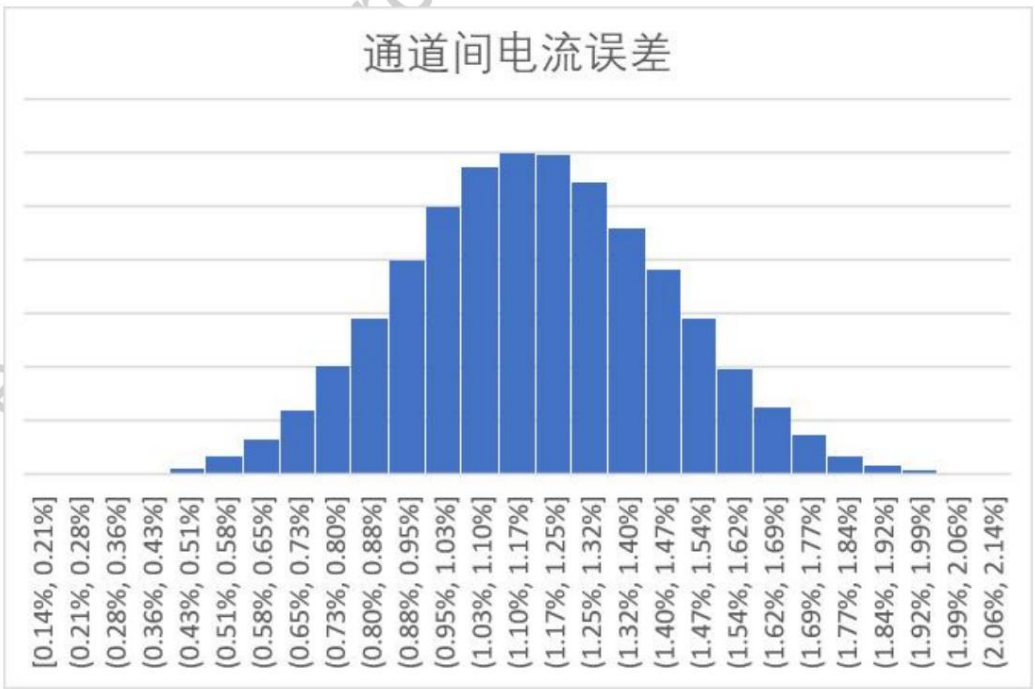
9 Typical characteristic diagram

9.1 Constant current source accuracy test chart

9.1.1 Current Error Between Chips

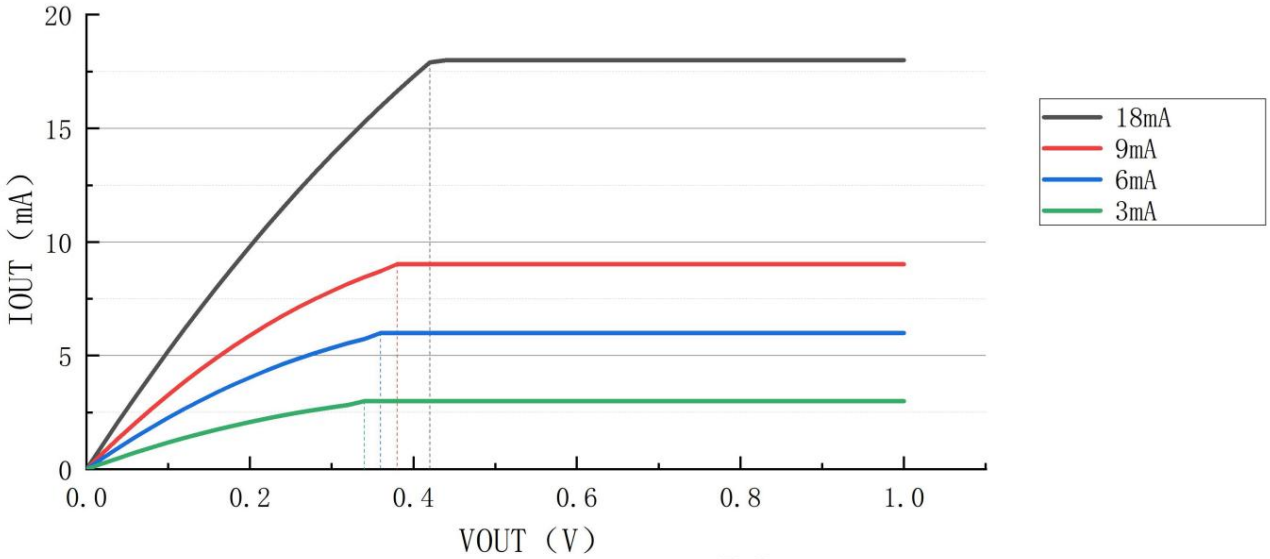


9.1.2 Current Error Between Channels



9.2 Constant current source inflection point

When DP3264S is applied to LED display design, the current difference between channels and even between chips is very small. This is due to the excellent constant current output characteristics of DP3264S: ÿ The maximum current between channels on the chip is less than ±2.0%, and the maximum current error between chips is less than ±2.0%; ÿ When the load voltage (Vout) changes, the stability of its output current is not affected, as shown in the following figure:



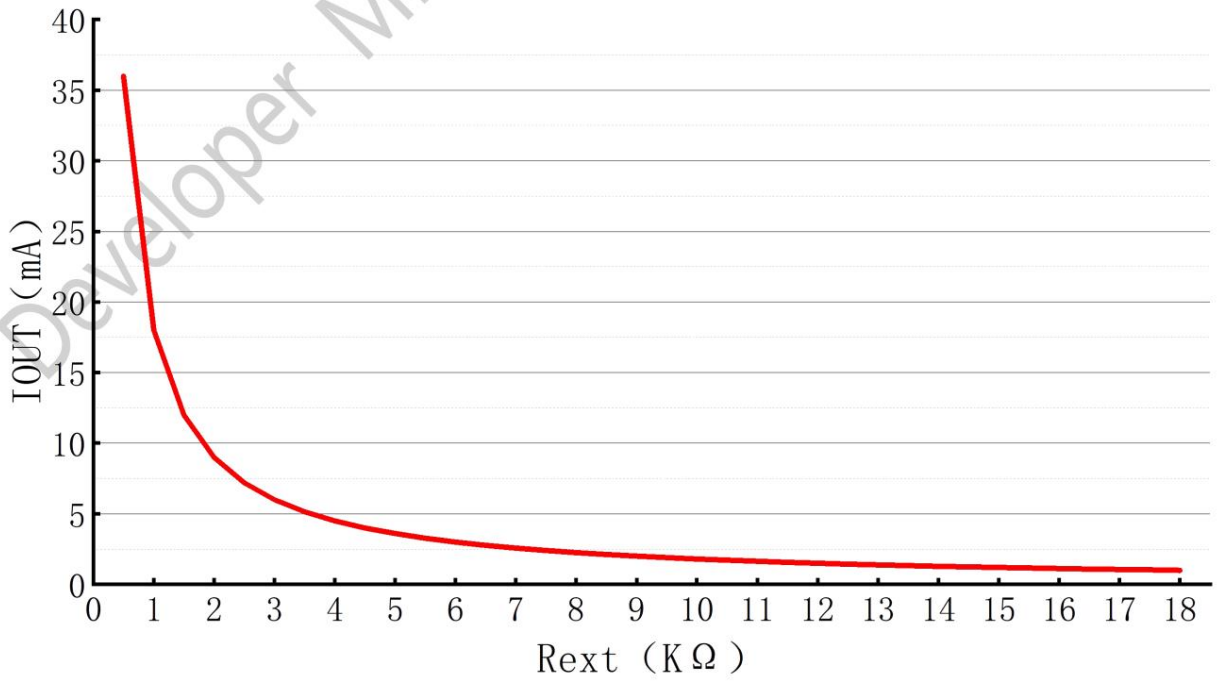
When VDD=3.5V-5.5V, the relationship curve between IOUT and VOUT

9.3 Adjusting the output current by external resistor

The output current value is calculated as follows:

$$= \frac{}{}, \quad \textbf{12.5\% ÿ IGAIN ÿ 200\%}$$

REXT in the formula is the resistance value of the chip 23PIN REXT port to ground. For example, when the current gain IGAIN = 100%, REXT = 1kÿ, the output current value can be calculated as 18mA.



IGAIN=100%, the relationship curve between REXT and Iout

10 Typical display effect samples

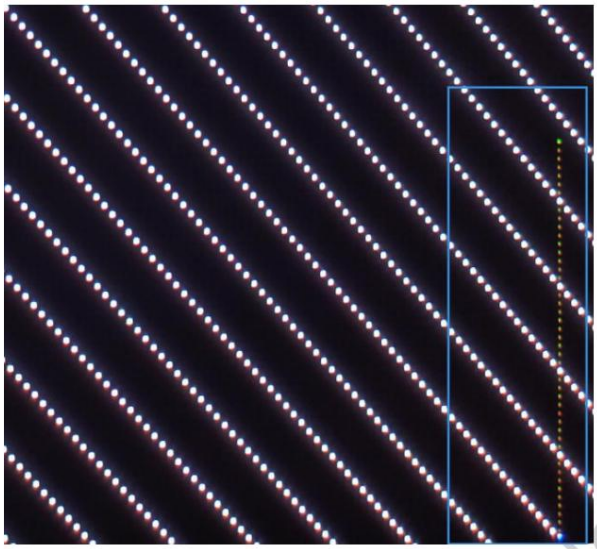
ÿ The specific display effect will be affected by the light board conditions and register parameters. The following test results are for reference only.

10.1 Display Effect

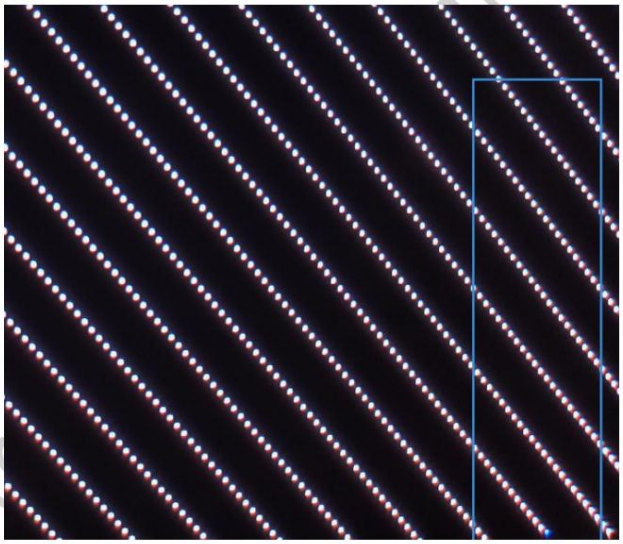
10.1.1 Remove open circuit bad point cross

The following is a comparison of the display effects before and after removing the open-circuit bad pixel cross. It can be

seen that: ÿ After the chip executes the open-circuit bad pixel cross removal function, the bad pixel cross can be removed well and the display effect can be optimized.



Remove the open circuit bad pixel before the cross display effect



Display effect after removing the open circuit bad pixel cross

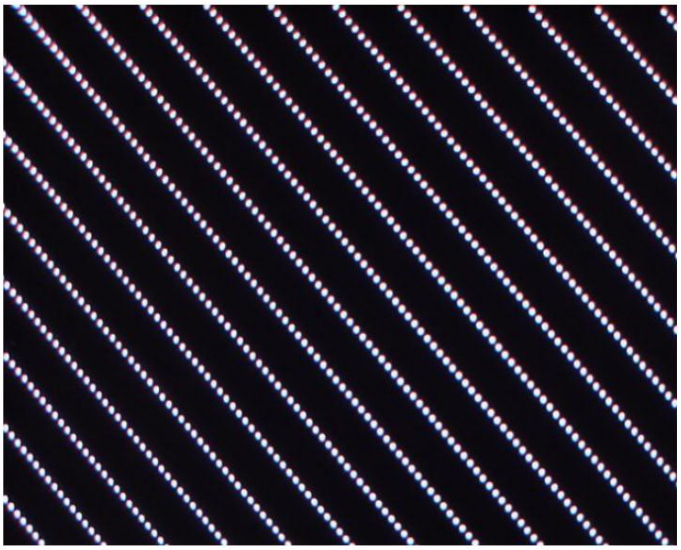
10.1.2 Removing ghosting and band-brightening effects

Below is the effect of removing ghosting and no bright band, you can see:

ÿ Ghosting and text ghosting problems cannot be observed under oblique scanning.

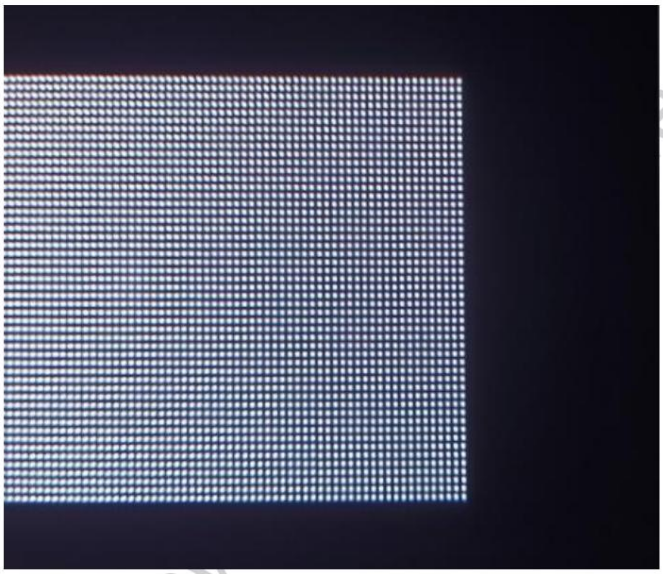
ÿ The highlight block is bright, and the oblique scanning and superimposed highlight block bright test display effect is very good.

ÿ The chip shows good display effect.

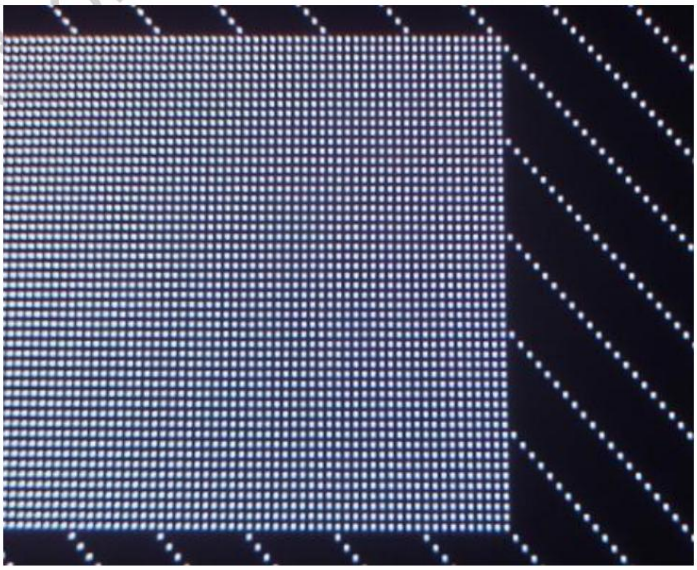


Ghost test display effect under oblique scanning

Text ghosting test display effect



Highlight block with bright test display effect



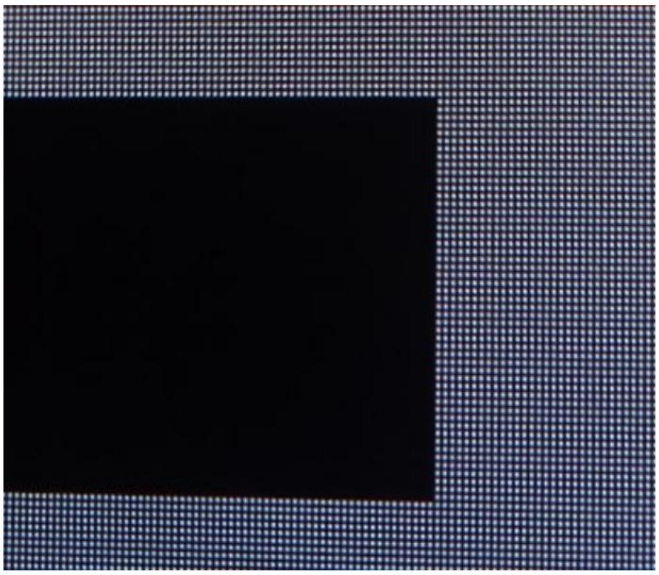
Oblique scanning superimposed highlight block with bright test display effect

10.1.3 Optimization of high and low gray interference and coupling display adverse effects

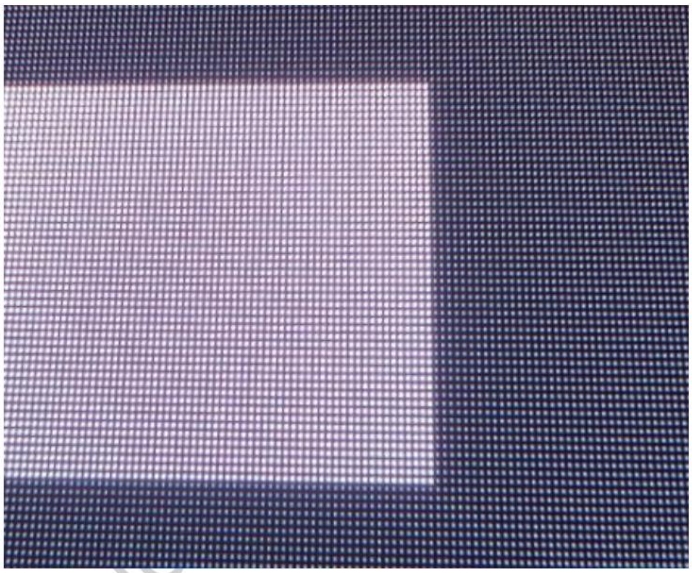
The following figure shows the optimization effect of high and low gray interference and coupling display adverse effects. You can see:

ÿ Neither the black block low-gray coupling nor the white block low-gray coupling can be felt.

ÿ The chip shows good display effect.



Black block low gray coupling test display effect



White block low gray coupling test display effect

11 Instructions and Registers

11.1 Register Instructions

Command name	THE	describe
DATA_LATCH	1	Latch 16bit data and send it to SRAM
VSYNC	3	Update display data
WR_CFG	5	Write register
PRE_ACT	14	Write enable

11.2 Data Instructions

Data sending order	OK	aisle
1	Line 0	Channel 15ÿOUT15ÿ
2		Channel 14ÿOUT14ÿ
……		……
16		Channel 0ÿOUT0ÿ
17	Line 1	Channel 15ÿOUT15ÿ
18		Channel 14ÿOUT14ÿ
……		……
32		Channel 0ÿOUT0ÿ
……		
497	Line 63	Channel 15ÿOUT15ÿ
498		Channel 14ÿOUT14ÿ
……		……
512		Channel 0ÿOUT0ÿ

11.3 Write Register

First send PRE_ACT, then execute WR_CFG, LE is 5 DCLK width, the first 8 bits input are the register address bits, and the last 8 bits input are the register address bits. is the data bit corresponding to the register address.

For example:

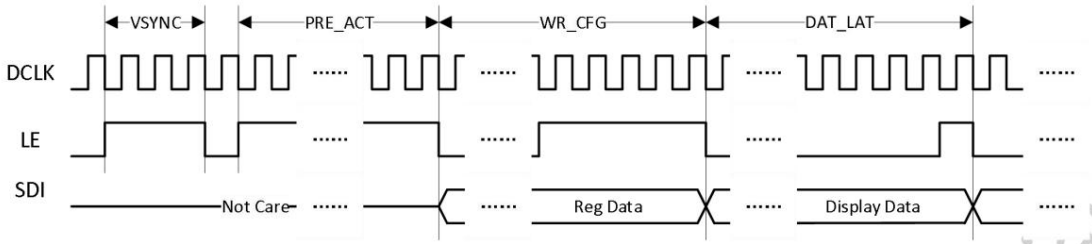
{A7, A6, A5, A4, A3, A2, A1, A0} = 8'b0000_0111;

{D7, D6, D5, D4, D3, D2, D1, D0}=8'b1001_1101;

This means setting register 0x07 (8'b0000_0111) to 8'b1001_1101.

11.4 How to send register signals

The specific driving method is as follows:



As shown in the figure above, the order of sending instructions

and data in each frame is:

1. Send VSYNC. 2. Send

PRE_ACT. 3. Send WR_CFG to write register configuration. Each frame can only write the register value of one address, and 13 frames are required to complete the refresh of all registers (a total of 13

4. Send DAT_LAT several times and write display data with

SDI. 5. The display data transmission bit is 16 bits, and the DP3264 chip only

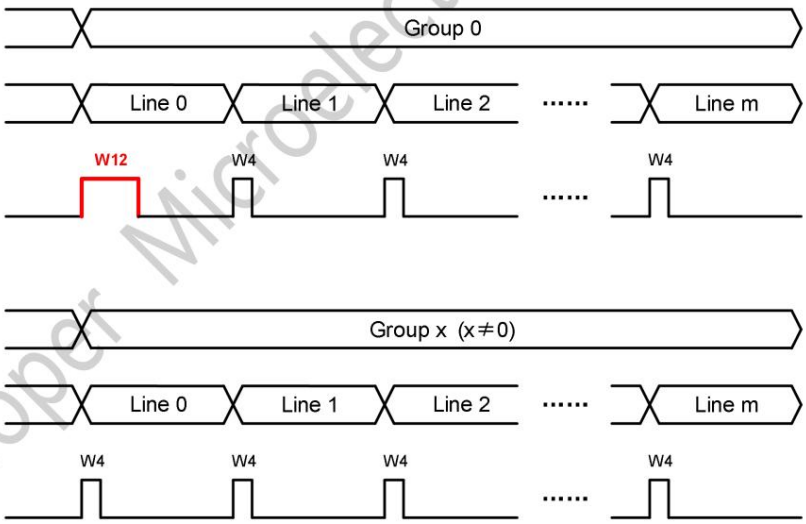
receives the lower 14 bits of the transmission data.

11.5 ROW signal transmission method

DP3264 integrates an on-chip GCLK generation circuit, which changes the OE signal of the general constant current chip to the ROW signal.

The rising edge indicates the beginning of a row of display. There are two types of high level widths of ROW:

1. W12: represents the high level width of ROW is 12 DCLK width
2. W4: represents the high level width of ROW is 4 DCLK widths

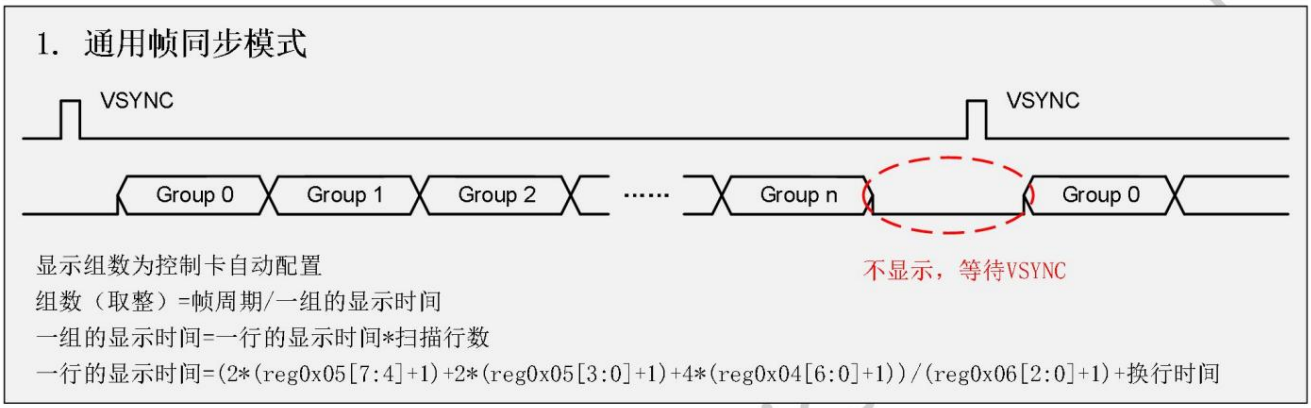


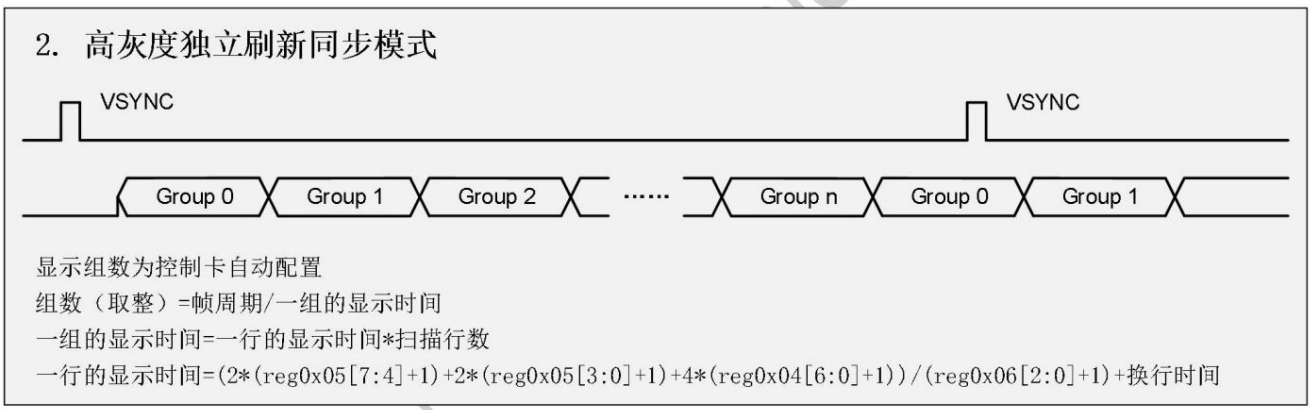
As shown in the figure above, when sending ROW signals, only the first row (Line 0) of the first group (Group 0) needs to send the ROW signal of W12, and the other ROW signals are

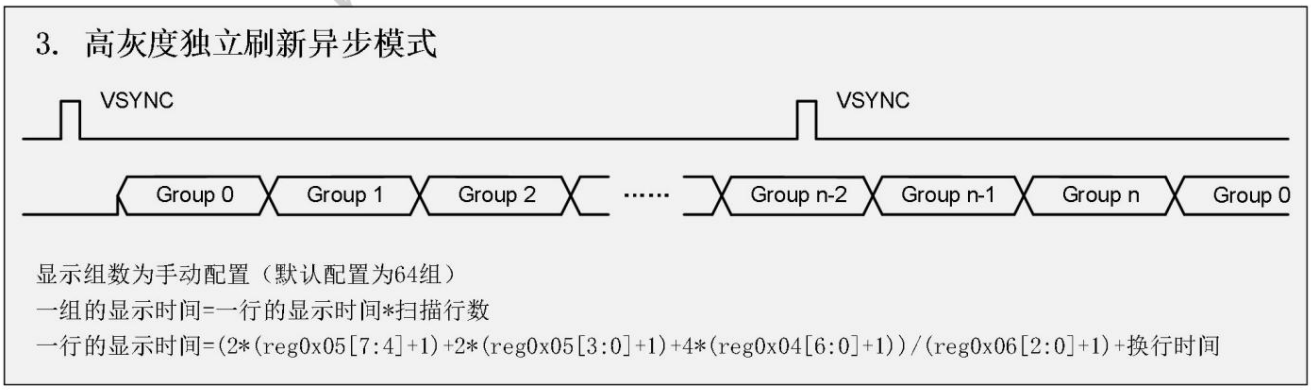
Send as W4.

11.6 PWM Display Mode

DP3264 integrates three PWM display modes: 1. General frame synchronization mode 2. High gray data independent refresh synchronization mode 3. High gray data independent refresh asynchronous mode In the high gray data independent refresh working mode, the black field time between frames in the general frame synchronization mode is eliminated due to the independent high refresh of high gray data, which can bring better photo effects.







11.6.1 General frame synchronization mode

The working mode and related configuration

are as follows: 1. Configure reg0x0c[7:6] = 0, set the PWM display mode to the general frame synchronization mode 2.

Calculate the number of DCLKs per line according to the formula 3.

Configure the number of display data groups, reg0x03[6:0] = refresh rate/frame rate-1 (supports a maximum of 64 groups of data, and registers are configured for more than 64 groups)

3. After VSYNC, display the first line (Line 0) of group 1 (Group 0) 4. After the current frame

of data is displayed, stop displaying until the next VSYNC arrives

11.6.2 High Gray Independent Refresh Synchronous Mode

The working mode and related

configuration are as follows: 1. Configure reg0x0c[7:6]=2, set the PWM display mode to high gray data independent refresh frame

synchronization mode 2. Calculate the number of DCLKs for each

line according to the formula 3. Configure the number of display data groups

according to the general frame synchronization mode: Number of display data groups = round(1/frame rate/

(number of row scans*display time of each line)) reg0x03[6:0]=number of display data groups-1 (maximum support 64 groups of data, exceeding 64 groups of registers, maximum visual refresh 3840)

4. ROW is sent continuously at a fixed display frequency without interruption. The frequency of ROW is independent of VSYNC.

The frequency of the ROW signal = 1/the display time of one row = 1/the time between two ROW rising edges

5. Group 0, row 0 sends ROW signal W12, otherwise sends ROW signal W4

There is only one W12 for each (number of groups * number of rows scanned) ROW signals, and it keeps circulating in this way.

Note: 1.

The VSYNC and ROW signals are asynchronously designed, and you only need to repeatedly send the ROW signal according to the Group's requirements. Even if VSYNC and Group

The overlap of ROW signals will not have any impact.

2. Please set the register GROUP_NUM (address reg0x03[6:0]) according to the minimum number of groups that can be sent. For example, if the shortest frame is 16ms, and each group

is 0.49ms, then the number of groups = 16/0.49 = 32.65. In this case, it should be rounded down to 32, and the register configuration should be set to 31 (actually displaying 32 groups).

11.6.3 High gray independent refresh asynchronous mode

The working mode and related

configuration are: 1. Configure reg0x0c[7:6]=3, set the PWM display mode to high gray data independent refresh asynchronous

mode 2. The number of DCLKs for each line is calculated

according to the formula 3. The number of display data groups is manually configured, the default is 64 groups (reg0x03[6:0]=7'h3f), and the maximum supports only 64 groups.

4. ROW is sent continuously at a fixed display frequency without interruption. The frequency of ROW is independent of VSYNC.

The frequency of the ROW signal = 1/the display time of one row = 1/the time between two ROW rising edges

5. Group 0, row 0 sends ROW signal W12, otherwise sends ROW signal W4

For each (number of groups (according to the register configuration value) * number of row scans) ROW signal, there is only one W12, and it keeps looping in this way. There is no limit to the number of loops in one

frame time, and the refresh rate can be greater than 3840. **Note:** The main differences between

the high

gray data independent refresh frame synchronization mode and the asynchronous mode are: 1. High gray data

independent refresh frame synchronization mode: the number of display data groups is automatically configured according to the display frame

time 2. High gray data independent refresh asynchronous mode: the number of display data groups can be manually configured

11.7 PWM display configuration

11.7.1 Row Scan Number Configuration

DP3264 supports up to 64 line scans, configured as reg0x02[5:0] = line scan number - 1

11.7.2 Row Grayscale Configuration

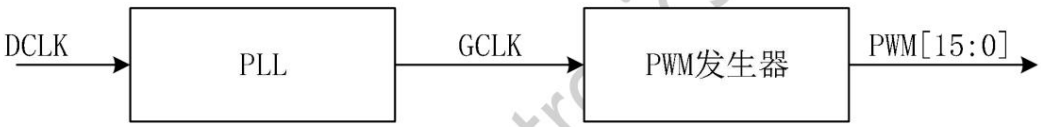
reg0x04[6:0] represents the PWM display length of a line. The PWM display length of a line = 4*(reg0x04[6:0]+1), and the maximum supported is 64X4=256. For example, if the gray level of the configuration line is 128, then set reg0x04[6:0]=7'h1f=31

11.7.3 PWM Display Group Configuration

reg0x03[6:0] represents the number of PWM display groups, PWM display group number = reg0x03[6:0]+1, the maximum supported group number is 64 groups. In frame synchronization mode, PWM display group number = refresh rate/frame rate, configuration reg0x03[6:0] = refresh rate/frame rate-1 (maximum support 64 groups of data, exceeding the 64 groups of registers)

In asynchronous mode, PWM display groups can be configured independently (regardless of refresh rate)

11.7.4 Internal Grayscale Clock Configuration



The DP3264 on-chip integrated PLL generates the grayscale clock GCLK. The relevant calculation formula is as follows:

FGCLK=FDCLK*(reg0x06[2:0]+1)

11.7.5 PWM Grayscale and Gamma Generation

PWM grayscale number (maximum value) = row grayscale number * PWM display group = 4 * (reg0x04[6:0] + 1) * (reg0x03[6:0] + 1) - 1 For example:

reg0x04[6:0] = 7'h3f, reg0x03[6:0] = 7'h3f

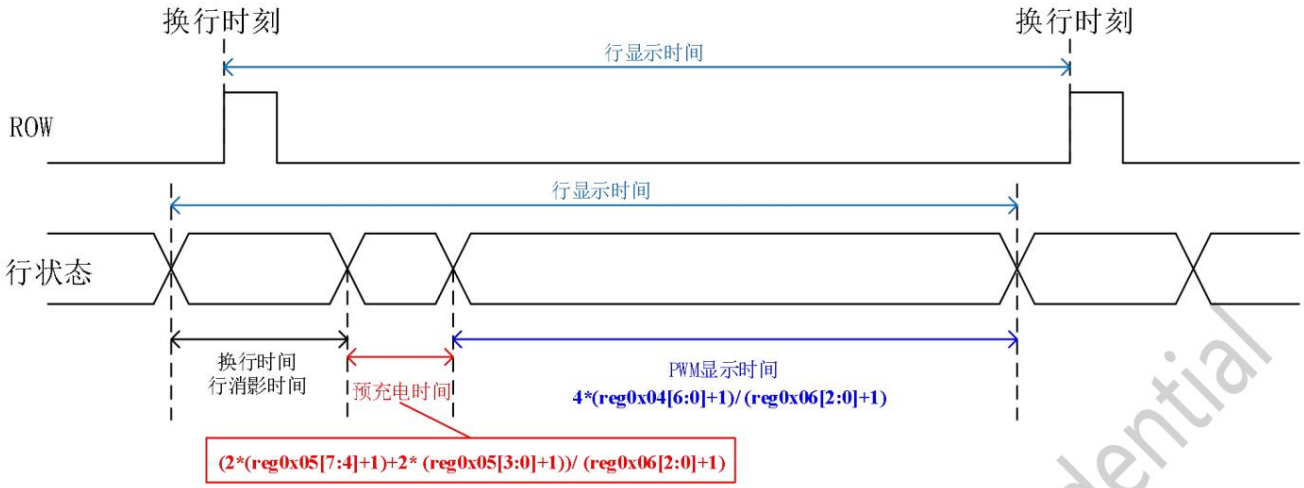
PWM grayscale number (maximum value) = 4*(63+1)*(63+1)-1=16383=14bit

Gamma can be calculated and generated according to the PWM grayscale level (maximum value) (this part is generated by the control card manufacturer according to its own gamma generation formula)

The maximum grayscale level supported by the chip is 14 bits (the lower 14 bits are valid)

11.7.6 Calculation of row display time for each row

The display time of each line is expressed by the number of DCLKs. The calculation formula is: (2*(reg0x05[7:4]+1)+2*(reg0x05[3:0]+1)+4*(reg0x04[6:0]+1))/(reg0x06[2:0]+1)+line break time. Note: The result of the above formula is rounded to the nearest integer.



11.8 Open Circuit Detection and Bad Pixel Removal

Check [Remove bad pixels]: reg0x0c[1]=1;

Uncheck [Remove bad pixels]: reg0x0c[1]=0

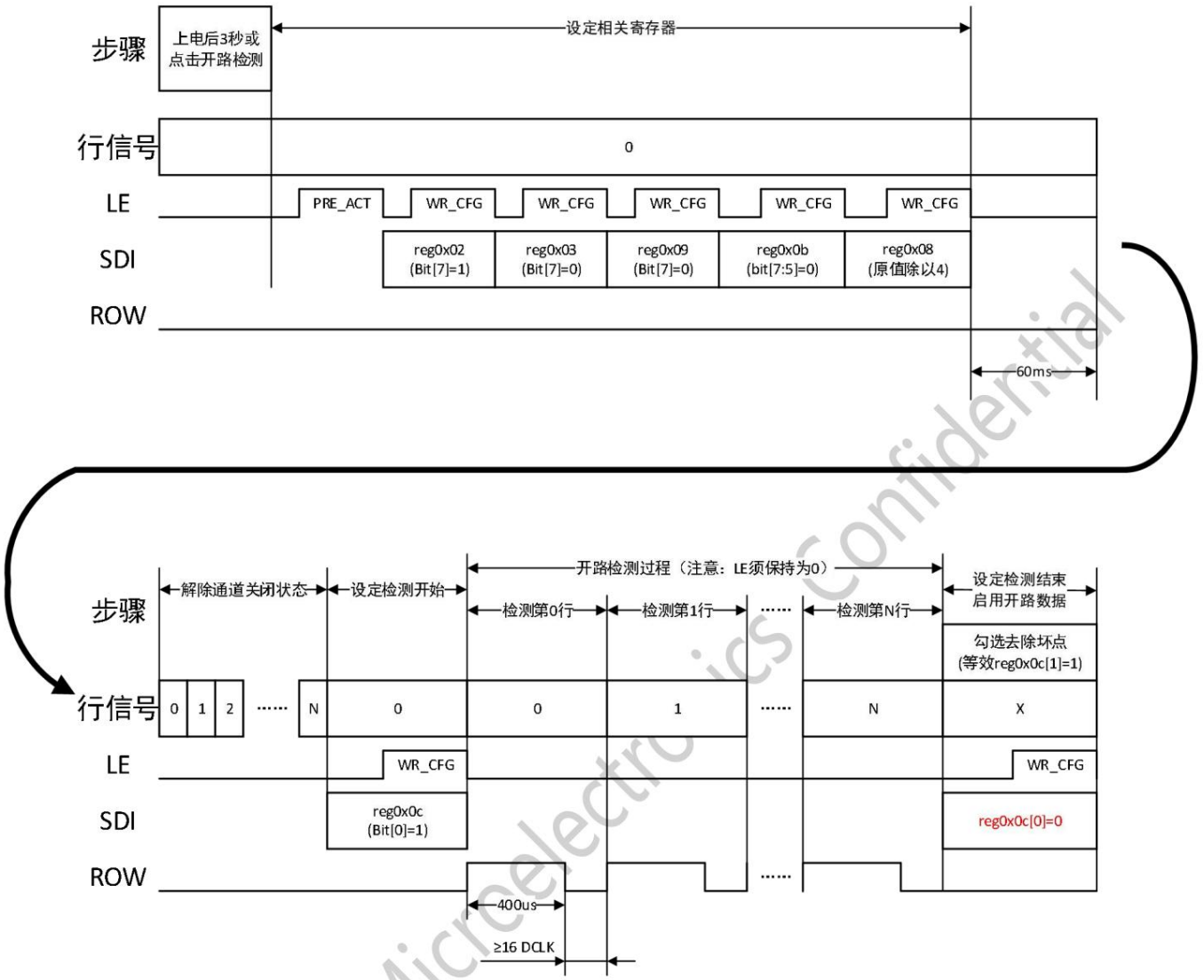
Open circuit detection timing:

1. Execute open circuit detection 3 seconds after power-on or after clicking open circuit detection.
2. Configure reg0x02[7]=1, reg0x03[7]=0 (enable open circuit detection mode)

   Configure reg0x0b[7:5]=0 (configure the constant current inflection point to the lowest)

   Configure reg0x08[7:0] to shift right by two bits and fill the high bits with 0 (configure the output current to be 25% of the normal current)
3. The line signal switches to line 0, and all line signals are stopped, waiting for one frame time (60ms)
4. Change the row signal, quickly scan from row 0 to the last row, and then return to row 0 (this step is mainly to avoid the existence of some row driver chips output channel is closed).
5. Configure reg0x0c[0]=1 (open circuit detection mode is enabled)
6. Send Row signal, that is, first set Row to high, then set ROW to low, the high level time (recommended 400us) is required to detect a row

   The low level time (recommended ÿ16 DCLK) is the data acquisition and latching time.
7. Line wrapping: Execute step 6 as many times as the number of lines to be scanned. It is recommended to align the line wrapping moment with the rising edge of ROW.
8. After the detection is completed, configure reg0x0c[0]=0 (turn off the open circuit detection mode) and reg0x0c[1]=1 (when [Remove bad pixels] is checked).
9. During the open circuit detection, LE=0, DCLK is sent normally and continuously (at least 128 DCLKs are guaranteed between two ROWs).



11.9 Registers

register	Register Function Name	Register function description and default value
0x02		Rÿ2A Gÿ2A Bÿ2A
7	OPDET_EN_A1	OPDET_EN_A1 is high effective; it needs to be coordinated with OPDET_EN_A2 and OPDET_EN_A3
6		Reserved
5:0	LINE_SET<5:0>	Number of scan lines = LINE_SET + 1
0x03		Rÿ3F Gÿ3F Bÿ3F
7	OPDET_EN_A2	OPDET_EN_A2 is low effective; it needs to be coordinated with OPDET_EN_A1 and OPDET_EN_A3
6:0	GROUP_SET<6:0>	Display refresh rate = (REG0F<7>*128+REG03<6:0>+1)
0x04		Rÿ20 Gÿ20 Bÿ20
7		Reserved
6:0	PWM_WIDTH<6:0>	Row PWM width = 4*(PWM_WIDTH + 1)
0x05		Rÿ34 Gÿ34 Bÿ34
7:3	DISSHD_TIME_1<3:0>	Shadow Moment - Level 0~Level 15, a total of 16 levels, the default value is 0
2:0	DISSHD_TIME_2<3:0>	Disappearance time - Level 0~Level 15, 16 levels in total
0x06		Rÿ42 Gÿ42 Bÿ42
7:3	DECOUP_RAT<4:0>	Coupling optimization coefficient
2:0	PLL_DIV<2:0>	fGCLK=fDCLK*(PLL_DIV +1)
0x07		Rÿ00 Gÿ00 Bÿ00
7	Gamma_COARSE_EN	Gamma coarse adjustment switch -1: Coarse adjustment enabled 0: Coarse adjustment disabled
6:4	Gamma_COARSE<2:0>	Gamma coarse adjustment level - 0~7 levels, 8 levels in total
3	Gamma_FINE_EN	Gamma fine adjustment switch -1: Fine adjustment enabled 0: Fine adjustment disabled
2:0	Gamma_FINE<2:0>	Gamma fine-tuning level - 0~7 levels, 8 levels in total
0x08		Rÿ7F Gÿ7F Bÿ7F
7:0	IGAIN<7:0>	reg08[7:6] is the 50% increment of the current gain reg08[5:0]= round (128*IGAIN/(reg08[7:6]+1))-1
0x09		Rÿ60 Gÿ60 Bÿ60
7:4		Reserved
4:0	DECOUP_1<4:0>	Coupling optimization 1-0 level ~ level 31, a total of 32 levels
0x0a		RÿBE GÿBE BÿBE
7:6	DECOUP_ENHANCE<1:0>	Coupling optimization enhancement level - from 0 to 3, it decreases in sequence
5		Reserved
4	DISSHD_EN	Shadow level switch - On: 1 Off: 0
3	DECOUP_EN	Coupling Optimization Switch
2:1	PIT_OPT<1:0>	Low gray spot optimization - level 0~3, 4 levels in total, default is level 3
0	LG_ENHANCE	Low gray display effect enhancement switch
0x0b		Rÿ28 Gÿ30 Bÿ31

7:5	CORNER <2:0>	Constant current output inflection point level 0: Low transition (0.18 V - 0.28 V) corresponding current range is 0.5mA~18mA 1: Low transition (0.2 V - 0.3 V) corresponding current range is 0.5mA~21mA 2: Low transition (0.23 V - 0.4 V) corresponding current range is 0.5mA~25mA 3: Low transition (0.26 V - 0.5 V) corresponding current range is 0.5mA~30mA 4: Normal (0.34 V - 0.6 V) The corresponding current range is 0.5mA~36mA
4:0	DISSHD_LEVEL<4:0>	Shadow Vanishing Level, Level 0~Level 31, 32 Levels in Total
0x0c		Rÿ90 Gÿ90 Bÿ90
7:6	SYNC_MODE<1:0>	0/1: Frame synchronization mode 2: High gray data independent refresh synchronization mode 3: High gray data independent refresh asynchronous mode
5:4	LP_MODE<1:0>	Energy saving mode 0: Dynamic energy saving 1: Dynamic energy saving + black screen energy saving mode 1-performance priority 2: Dynamic energy saving + black screen energy saving mode 2 - low power consumption first 3: Dynamic energy saving + black screen energy saving mode 3-extremely low power consumption
3:2		Reserved
1	RM_OP	Remove bad pixel function switch
0	OPT_EN	If both conditions OPDET_EN_A1 and OPDET_EN_A2 are met, open OPDET_EN and enter Open circuit detection mode
0x0d		Rÿ08 Gÿ12 Bÿ18
7:5		Reserved
4:0	DECOUP_LEVEL<4:0>	Coupling optimization level, level 0~level 31, a total of 32 levels
0x0e		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x0f		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x10		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x11		Rÿ00 Gÿ00 Bÿ00
7	OPEN_EN_B	OPEN_EN_B High effective
6:0		Reserved
0x12		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x13		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x14		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x15		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x16		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved
0x17		Rÿ00 Gÿ00 Bÿ00
7:0		Reserved

12 Package heat dissipation power (PD)

The maximum heat dissipation power of the package is given by the formula $P_{D(max)} = \frac{(T_j - T_a)}{R_{th(ja)}}$ To decide

When all 16 channels are turned on, the actual power is:

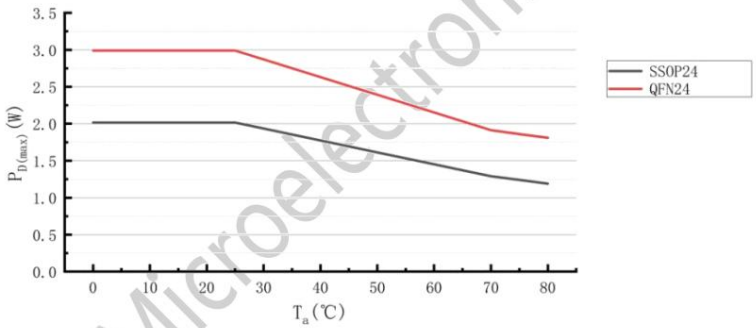
PD(act) = IDD * VDD + IOUT * Duty * VDS * 16

To ensure PD(act)≤PD(max), the relationship between the maximum output current and duty cycle is:

$$I_{OUT(max)} = \frac{\frac{T_j - T_a}{R_{th(j-a)}} - (I_{DD} * V_{DD})}{V_{DS} * Duty * 16}$$

Where Tj is the junction temperature (Tj=150℃), Ta is the ambient temperature, VDS is the constant current output port voltage, Duty is the duty cycle, and Rth(ja) is the thermal resistance of the package.

Encapsulation	Rth(j-a)(℃/W)	PD(max)(W)
QSOP24	62	2.01
QFN24	41.8	2.99



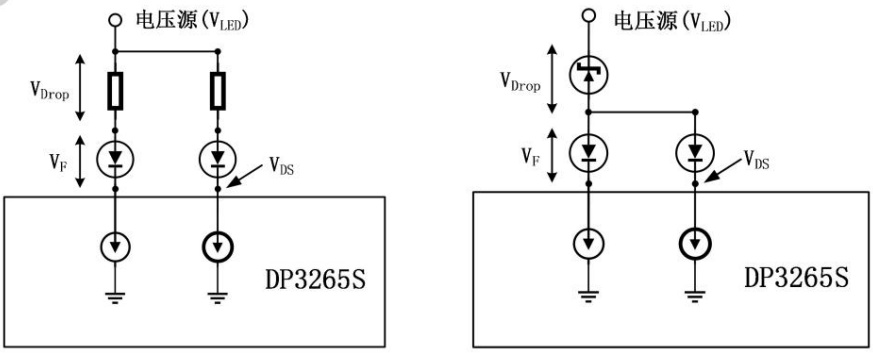
13 Load terminal voltage (VLED)

In order to optimize the heat dissipation capacity of the package, the recommended optimal operating range of the output voltage (VDS) is 0.3V to 1.0V (IOUT = 0.5 to 36mA).

VDS=VLED-VF and VLED=5V. At this time, too high output voltage (VDS) may cause PD(act)≤PD(max). In this case, it is recommended to use a lower

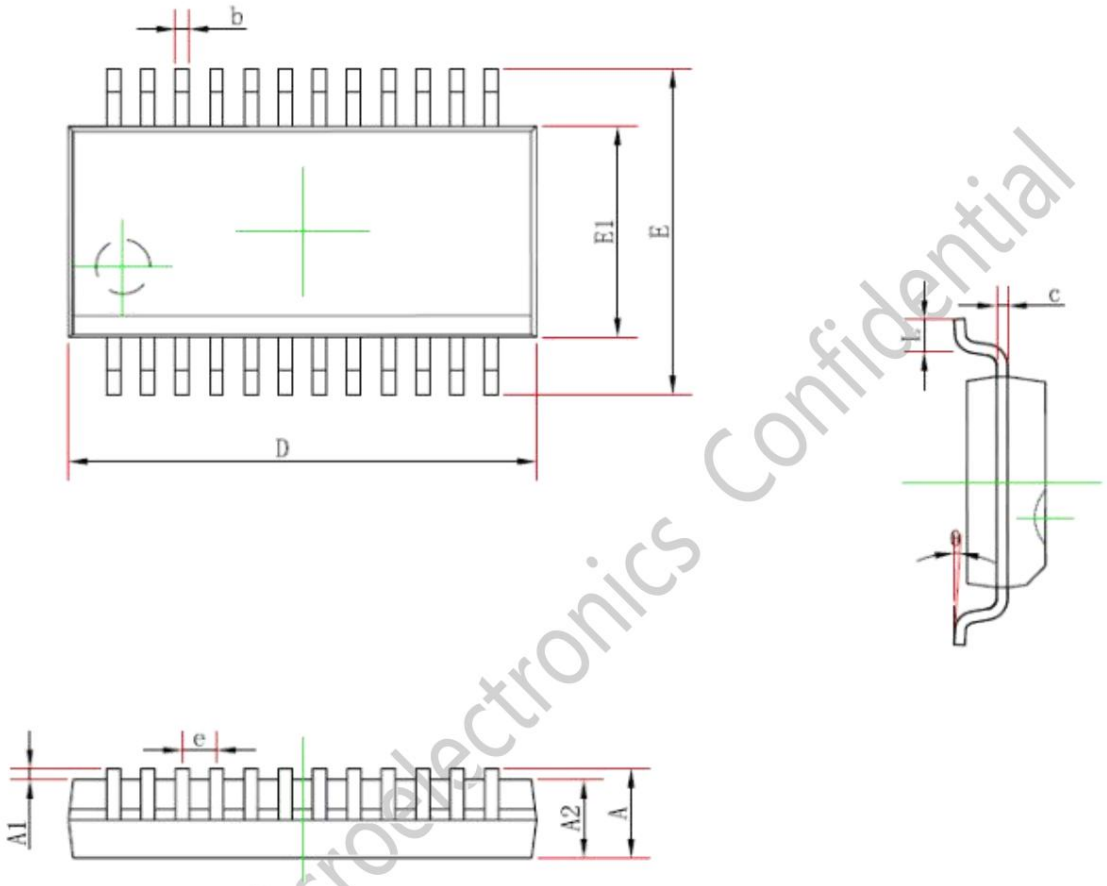
VLED voltage supply, can also use external series resistor or voltage regulator as VDROP. At this time, VDS = (VLED-VF)-VDROP, achieving the effect of reducing the input voltage (VDS) value.

The application diagram of external series resistor or voltage regulator can refer to the figure below.



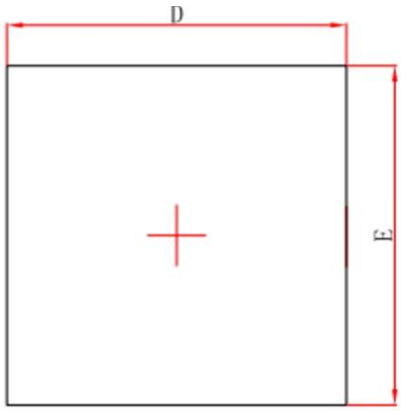
14 Packaging Information

ÿ QSOP24 plastic package specification diagram

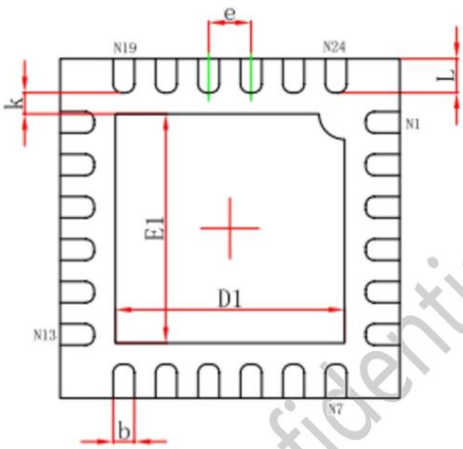


	Millimeter (mm)	
	Minimum value (Min)	Maximum value (Max)
A	–	1.95
A1	0.05	0.35
A2	1.05	–
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
AND	5.6	6.5
and	0.635TYP	
L	0.3	1.5
i	0°	10°

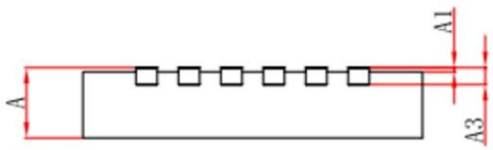
ÿ QFN24 plastic package specification diagram



Top View



Bottom View



Side View

	Millimeter (mm)	
	Minimum value	Maximum value (Max)
A	(Min) 0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF	
D	3.924	4.076
AND	3.924	4.076
D1	2.6	2.8
E1	2.6	2.8
k	0.20MIN	
b	0.200	0.300
and	0.500TYP	
L	0.324	0.476

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